

A Simple Class A JFET Operational Amplifier

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The schematic shown in Figure 1 is that of an operational amplifier constructed using individual (discrete) junction field effect transistors (JFET). While this circuit is very simple, it is a very high performance circuit and not only measure well, but has received much critical acclaim for its sonic quality. Many thousands of these circuits are in use today in recording studios and mastering facilities world wide.

The circuit uses a very specific JFET family from Toshiba: the 2SK170/2SJ74 devices. These JFETs are high transconductance devices. The 2SK170 is an N-channel JFET and the 2SJ74 is a P-channel JFET with complementary specifications. While these two are not perfectly matched complementary devices, they are very close and can be used as such. In certain applications, matching and grading of these parts is needed.

The input stage of this amplifier is comprised of a differential amplifier (Q1 & Q2) with a constant-current regulator (Q3) (CCR) used in place of a “tail” resistor. Normally a tail resistor is used to set the operating point for the two halves of the diff-amp. For example, if Q3 was replaced with a 10k ohm resistor, the current flow through this resistor to the diff-amp would be $24/10,000$ or 2.4 milliamps. Since the two halves of the diff-amp share this common resistor, the current flow through either Q1 or Q2 will be $2.4/2$ or 1.2 ma. When a CCR is used in place of the resistor, it is selected or configured to provide the current needed to operate both JFETs at the proper operating point. More on this later.

The reason for using a current source instead of a tail resistor is simply because it provides a higher impedance at the sources of the diff-amp that we could practically achieve with a resistor connected to a negative power source. Because the common mode rejection ratio of a diff-amp stage is a directly proportionate to the impedance of the tail resistor, using a CCR results in improved common mode rejection performance. While there are other CCR topologies that provide even higher dynamic impedance, one of the simple design of a single JFET was chosen because of its simplicity. The single JFET CCR provides a suitably high dynamic load and low noise performance. The CCR is biased to the desired operating point by selecting R2 for the desired current flow through the JFET. We talk more about this in a moment as well.

A single-ended, inverting output is taken from the input stage diff-amp and direct coupled to Q6 which provides the final voltage gain for the circuit. An active drain load (Q4) is used in order to achieve the highest gain possible from this last voltage amplifier (LVA). R7 provides some source degeneration and helps to stabilize this stage and provide more linear operation. R7 also increases the DC voltage present at the source of Q6, which allows a larger resistors to be used for R1.

The drains of Q6 and Q4 are sitting at (or very near) zero VDC, allowing the output stage to be direct coupled to the point while still keeping the output of the amplifier a zero

VDC. Both R5 and R7 are operating as source followers and provide no voltage gain. If R3 was made zero ohms, then the output stage will be fully Class A. Increasing the value of R3 from zero ohms will move the operating point of the output stage away from Class A. With the 10 ohm value shown, the output stage is still operating Class A up to a reasonable output current, and the output stage runs a little bit cooler than it would without the 10 ohm resistor. The source resistors (R5 & R6) in the output stage provide some degeneration to help stabilize the output stage, and some short-circuit protection.

The 2SK170/2SJ74 JFET family is factory sorted into three current ranges (for I_{dss}). The GR series (2.6-6.5 ma), the BL series (6-12 ma) and the V series (10-20 ma). It is theoretically important to select the proper range for the devices used in this opamp. For example, Q1 and Q2 should be GR series devices, Q3, Q4, and Q6 should be BL series, Q5 and Q7 should be V series. In reality, it may be better to order a large number of BL series parts and then sort them as to their exact I_{dss} (yes, you'll have to measure each one). You can then use the lower current parts in place of the GR series and the highest current part in place of the V series. You could also select Q5 and Q6 for matched V_{gs} (gate-source voltage) to provide near zero output DC offset, but this can be trimmed within a reasonable range with R8.

When it comes to selecting the I_{dss} of a given device, the idea is to use a CCR JFET that has approximately the same I_{dss} as the JFET to which it is connected. In the case of the differential amplifier, the CCR JFET (Q3) should have an I_{dss} equal to the sum of I_{dss} of the two differential amplifier JFETs (Q1 & Q2). For the LVA (Q6) the CCR (Q4) should have approximately the same I_{dss} as the LVA (Q6). The output stage JFETs should have matched I_{dss} and reasonably close V_{gs} , as discussed above.

With output loads above 600 ohms, the LVA (Q6) will clip before any other stage of this circuit. Since the 2SJ74 has a maximum drain-source voltage of 25 VDC, this opamp can not use power supply rail voltages greater than bipolar 24 VDC to increase the clipping point. With a bipolar 24 VDC, this opamp will produce a +24 dBu into loads above 600 ohms.

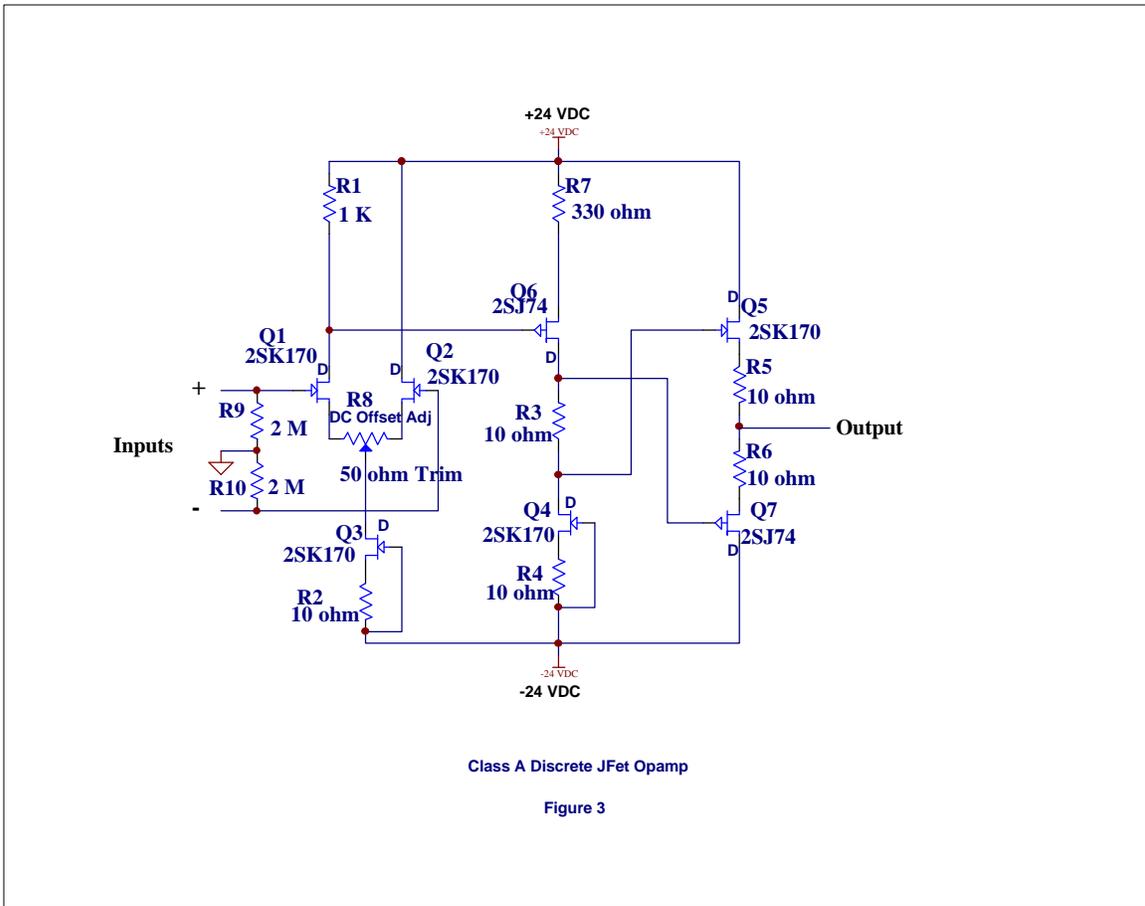


Figure 1